# CAPACITANCE TOPOLOGY FOR HIGH FREQUENCY MODELING OF BIPOLAR TRANSISTORS

**Alexandru A. Ciubotaru* and Ronald L. Carter**
**Department of Electrical Engineering, University of Texas at Arlington,**
**BOX 19016, Arlington, Texas 76019-0016**
***currently with National Semiconductor, Arlington, Texas, 76017**

## ABSTRACT

The standard SPICE Gummel-Poon model for bipolar transistors in the case of current crowding is inaccurate at high frequencies primarily due to the position of the capacitances. An improved distributed bipolar transistor model is developed, with fractions of both the depletion and the diffusion capacitances placed outside the base spreading resistance and the transistor junctions. The model is contrasted with the standard model by comparing the high frequency characteristics for an HBT.

## INTRODUCTION

The standard lumped-element implementation in SPICE of the Gummel-Poon model [1], [2] is a widely accepted circuit representation for the bipolar transistor. This model, however, introduces large errors at high frequencies and currents, primarily because it assumes a lumped one-dimensional device, and ignores the concentration of the diffusion capacitances at the periphery of the device caused by the current crowding effect. The model proposed in this paper is a simple modification of the standard SPICE Gummel-Poon model, which consists of placing fractions of both the depletion and the diffusion capacitances outside the current-dependent base spreading resistance and the transistor junctions. The dc accuracy of the original model is preserved, as well as its ability to account for second-order effects such as transit time modulation and excess phase shift in the base.

## DEVELOPMENT OF IMPROVED MODEL

For a single base contact and constant base sheet resistance across the transistor, the circuit configuration of a planar transistor structure with a stripe emitter geometry and constant cross-sectional area is shown in Fig. 1(a) ($W$ and $L$ are the device width and length, respectively, and $r_{Bi}$ is the base sheet resistance [3]).

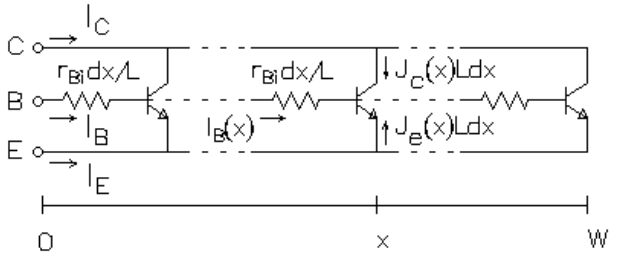


Fig. 1(a). Planar transistor with a single base contact, shown as a distributed structure.

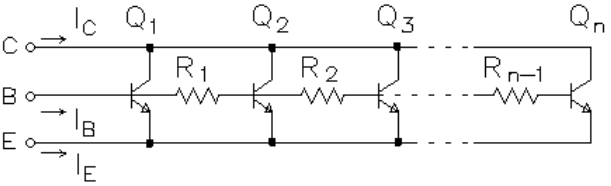


Fig. 1(b). Discrete approximation of planar transistor.

According to Fig. 1(a), the distributed transistor can be approximated by a cascade of discrete identical transistors and constant resistances, as shown in Fig. 1(b) [4], where the number of transistors is sufficiently large and $R_1 = \ldots = R_{n-1} = r_{Bi}\frac{W}{(n-1)L}$; no resistance appears in series with the base of transistor $Q_1$ because of the corresponding infinitesimal resistance in Fig. 1(a). The discrete transistors $Q_i$ of Fig. 1(b) have zero base resistance, and can be represented accurately according to the standard model as shown in Fig. 2 [1]. In Fig. 2, $C_{JEi}$ and $C_{JCi}$ are the depletion capacitances of the emitter and collector junctions, respectively, of transistor $Q_i$, and $C_{DEi}$ and $C_{DCi}$ are the

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corresponding diffusion capacitances [1]:

$$C_{DEi} = \frac{d(\tau_F I_{CCi})}{dV_{BEi}} = \tau_F \frac{dI_{CCi}}{dV_{BEi}} \quad (1)$$

$$C_{DCi} = \frac{d(\tau_R I_{ECi})}{dV_{BCi}} = \tau_R \frac{dI_{ECi}}{dV_{BCi}} \quad (2)$$

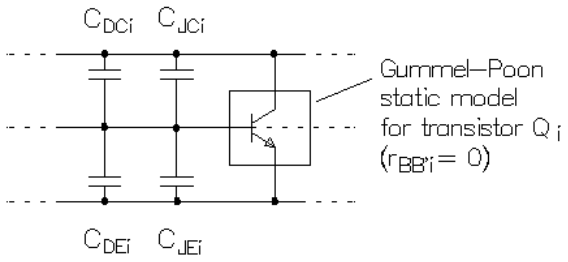


Fig. 2. Large-signal model for transistor $Q_i$, with the depletion and diffusion capacitances shown explicitly.

Assuming the transistor is in the forward active region, at sufficiently high dc base currents $I_B$ the voltage drop across the distributed base resistance causes the currents to flow mainly through the periphery of the device. This situation is illustrated in Fig. 3, which quantitatively shows the dc base currents of the first three transistors in the discrete circuit of Fig. 1(b) (for $n = 11$, which allows the simulation of the base spreading resistance in reasonable agreement with an exact analysis [5], $I_S = 10^{-26}$ A, $R_i = 3$ KΩ, $I_{Si} = I_S/n$, $\beta_{Fi} = \beta_F = 100$, $i = 1, \ldots, n$, and all the other transistor parameters assuming their SPICE default values). According to Fig. 3, for sufficiently large dc base currents, transistor $Q_1$ diverts almost all of the base current, and from Eq. (1) and the exponential dependence of $I_{CCi}$ [1], it follows that the diffusion capacitance $C_{DE1}$ is much larger than $(C_{DE2} + \ldots + C_{DE11})$. Therefore, in strong forward bias, a realistic model for a bipolar transistor should have the base-emitter diffusion capacitance connected directly between the base and emitter terminals, outside the base spreading resistance (for the same reason, the base-collector diffusion capacitance should be connected outside the base spreading resistance, in strong reverse bias).

The proposed capacitance topology for the SPICE model of a bipolar transistor is shown in Fig. 4. For similarity with the standard SPICE model, two new model parameters, $X_{CD}$ and $X_{CJ}$ ($0 \le X_{CD} \le 1$, $0 \le X_{CJ} \le 1$), represent the distributed effects due to the diffusion and depletion capacitances, respectively. In strong forward or reverse bias, $X_{CD} = 0$ ensures that $C_{DE}$ and $C_{DC}$ are actually connected between the external base and the emitter and collector nodes, respectively.

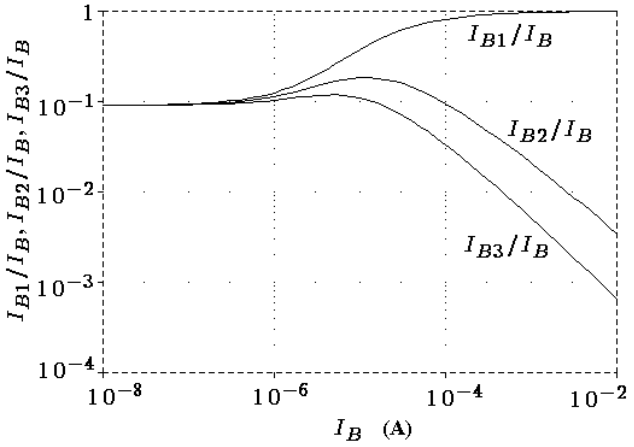


Fig. 3. $I_{B1}/I_B$, $I_{B2}/I_B$, and $I_{B3}/I_B$ as functions of dc base current $I_B$ ($n = 11$).

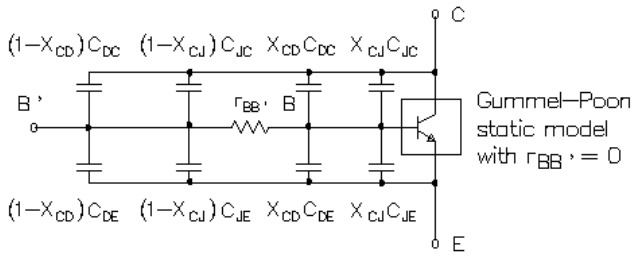


Fig. 4. Improved capacitance topology in the SPICE model of a bipolar transistor.

To illustrate the appropriateness of the proposed model of Fig. 4 and the inaccuracy of the classical SPICE model at high frequencies in strong forward bias, the two models have been ac simulated and compared with the reference structure of Fig. 1(b). Fig. 5 shows the magnitude of the input impedance in the common emitter configuration of the two models and the reference circuit, for constant $\tau_F = 0.1$ ns and $I_B = 100$ μA, and $X_{CD} = 0$ imposed for the proposed model of Fig. 4; the remaining parameters assumed the

values used in the simulation shown in Fig. 3. At high frequencies, the standard model is inaccurate due to the placement of the base-emitter diffusion capacitance (all other capacitances are zero); the model of Fig. 4 is a much better high-frequency representation of the distributed transistor operating at high currents.

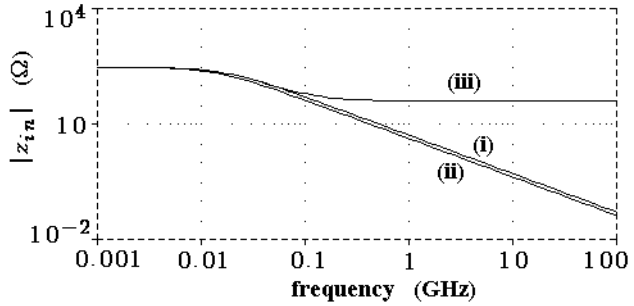


Fig. 5. Magnitude of CE input impedance of the circuits of Fig. 1(b) (i), Fig. 4 (ii), and the standard SPICE model (iii).

## RESULTS AND DISCUSSION

The model of Fig. 4 was further validated by comparing the measured and simulated S-parameters for an HBT in strong forward bias. The equivalent circuit of the HBT is shown in Fig. 6.

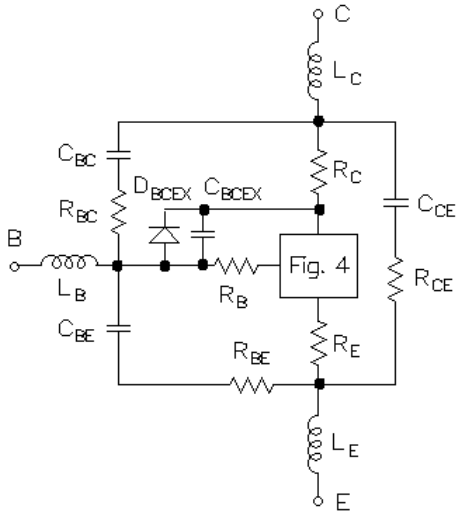


Fig. 6. Equivalent circuit of the measured HBT, including the pad and interconnection parasitics.

The model of Fig. 6 was implemented in the MNS simulator controlled by Hewlett-Packard's IC-CAP software [6], and the simulated S-parameters were fitted to the measured S-parameters, with the optimization variables being $X_{CD}$, $X_{CJ}$, and other parameters which could not be determined otherwise ($\tau_F$, $R_B$). For the dc bias conditions $V_{BE} = 1.43$ V, $V_{CB} = 1$ V, $I_B = 20.8\ \mu$A, $I_C = 1.4$ mA, the final values returned by the optimizer were $X_{CD} = 0.032$ (indicating that a large portion of the $C_{DE}$ has to be connected outside the base spreading resistance and the transistor junctions) and $X_{CJ} = 1$ (in agreement with the standard SPICE model topology).

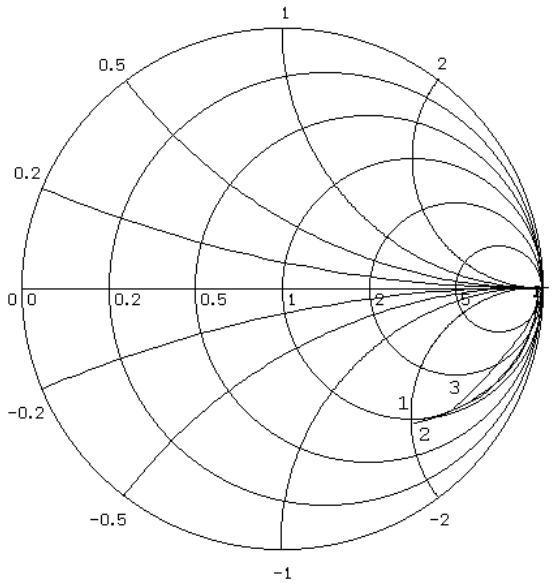


Fig. 7(a). $S_{11}$.

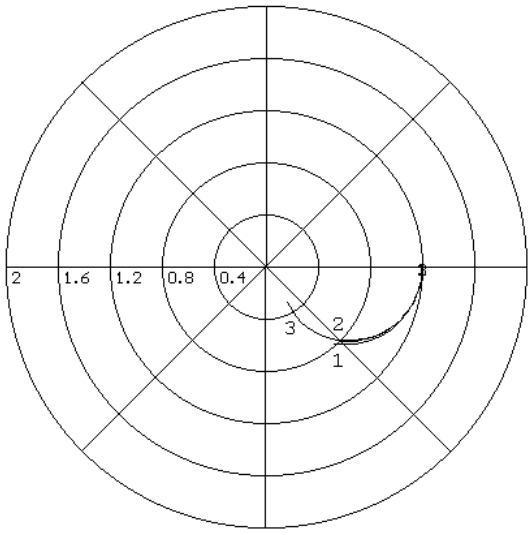


Fig. 7(b). $S_{21}$.

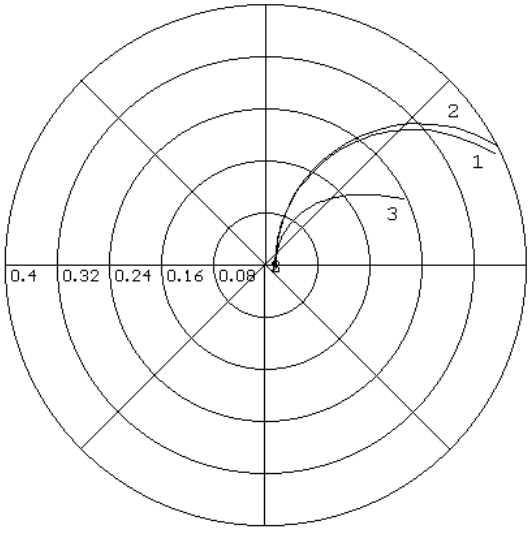


Fig. 7(c). $S_{12}$.

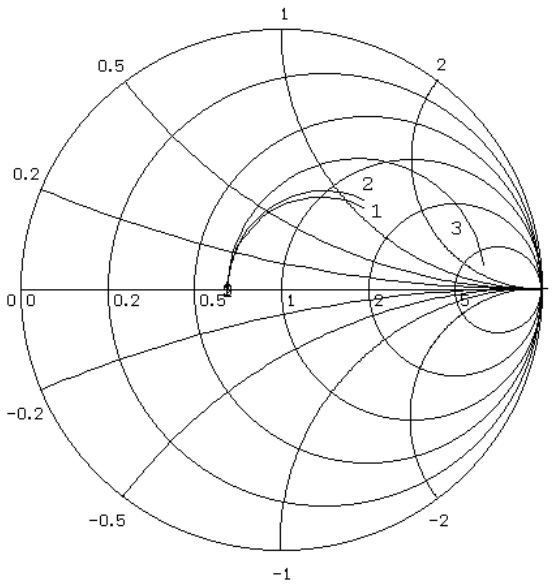


Fig. 7(d). $S_{22}$.

Fig. 7. Measured and simulated S-parameters of the HBT including the probe-pattern parasitics, in the frequency range $[46\ \text{MHz}, 25.87\ \text{GHz}]$ (1: measured, 2: simulated ($X_{CD} = 0.032$), 3: simulated ($X_{CD} = 1$)).

The important influence of the capacitance topology can also be inferred from Fig. 7(a)-(d), which shows the measured S-parameters of the HBT (under the above dc bias conditions) against the simulated S-parameters of its equivalent circuit (Fig. 6). To contrast the proposed model with the standard SPICE model, the simulation was performed in two cases, for $X_{CD} = 0.032$ (returned by the optimizer), and $X_{CD} = 1$ (used for the standard model). While the simulated S-parameters of the proposed model are in close agreement with the measured curves, the differences between the curves are relatively large in the case of the standard model. The model of Fig. 4 is a more accurate representation of the distributed effects in a bipolar transistor due to the diffusion and depletion capacitances.

## CONCLUSION

An improved capacitance topology for bipolar transistors has been proposed, with fractions of both the depletion and the diffusion capacitances placed outside the base spreading resistance and the transistor junctions. The new model has been validated by comparing its high-frequency characteristics with the characteristics of a reference structure and of the standard SPICE model, and also by comparing the high-frequency simulated and measured S-parameters for a heterojunction bipolar transistor.

## ACKNOWLEDGMENT

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